FPGA-Based Real-Time Simulation of Modular Multilevel Converter HVDC Systems

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Abstract: AC-HVDC-AC energy conversion systems using MMC (modular multilevel converters) are becoming popular to integrate distributed energy systems to the main grid. Such multilevel converters pose a serious problem for HIL (hardware in the loop) simulators required for control, protection design and testing due to the large number of cells that must be simulated individually using very small time steps. This paper demonstrates the advantages of using a very small time step to simulate a MMC topology. The MMC is implemented on FPGA (field-programmable gate array) to simulate fast transients with a time step of 250 ns. The AC network and HVDC bus is simulated on the PC, with a slower time step of 10 µs to 20 µs. The simulator architecture and the components simulated on the FPGA and on the PC will be discussed, as well as the method allowing the interconnection of this slow and fast system.

Key words: FPGA simulation, modular multi-level voltage source converters (MMC), MMC converter real-time simulation, HIL (hardware-in-the-loop).

1. Introduction

The global power system infrastructure is rapidly changing, from concentrated generation centers and EHV (extra high voltage) transmission grids towards increasingly distributed generation/distribution systems. This transformation mandates expanded use of power electronic devices: e.g. HVDC, FACTS and interfacing devices for DC and variable-frequency power sources (photovoltaic, wind generation). Power electronic converters have evolved rapidly, both in terms of available electronic switching devices and converter topologies. The evolution from thyristor-based converters to VSCs (voltage source converters) to MMCs (modular multilevel converters) [1, 2] has placed increasingly onerous demands on simulation technology, in particular real-time digital simulators. The challenge related to the simulation of VSCs, for example, is the very small time-step required to deal with relatively high carrier frequencies, and models have been developed that achieve accurate results using time-steps in the range of 20 to 50 microseconds [3, 4], typical of what may be achieved using standard INTEL/AMD multi-core processors. MMCs add to this challenge because of the large number of I/Os required monitoring the voltages of a large number of cells. In order to study higher frequency electromagnetic transients, the time step should be reduced even more [5].

Demonstration of real-time simulation and HIL (hardware in the loop) simulation for this topology was done in Refs. [1, 3]. At that time, the conclusion was that using a fifth order fixed step solver, with a time step of 20 µs, the model gives good enough results, whether to test the controller or to study system behaviour under certain tests; such as transformer saturation, unbalanced line, ground fault. Simulation was done using a regular Intel PC running Linux Redhat. OP5142 FPGA cards from Opal-RT were used in HIL to manage the analog and digital input/output. To do so, an FPGA card manages
communication between the CPU from the PC and hardware used to acquired physical signals. Since the model was simulated at 20 µs, which is relatively slow, an interpolation on the firing PWM signal was made to increase its resolution. Thought results are satisfying, even better and more accurate results could be obtained by lowering the time step used of the simulation. For instance, the digital-to-analog converter from the OP5142 has a refresh rate of 1.0 µs; using a time step this low would allow studying high speed transient phenomena, up to 50 to 100 kHz with a sampling frequency of 1 MHz (1 µs). Such a low time step value would eliminate the need for interpolation and facilitate the simulation of transients expected across each cell during natural rectification modes. Also, since the FPGA are already required for managing the IOs, they might be used to simulate part of the model as well.

In the system presented in this paper, a high-performance multirate/multiplatform simulation is proposed. The fast simulation will run on three different FPGAs at 250 ns, one FPGA per converter arm, and the slow part, AC and DC network, will run on CPU with a time step between 20 µs.

2. Modelling

2.1 Implementation of the MMC

A MMC is made of many identical cells first connected in series, forming a limb, then in parallel. Fig. 1 shows one cell and Fig. 2 shows the AC/DC converter [6, 7]. If the model is looked at with the standard approach, the size of the matrix to solve increases exponentially with the number of power switches. But by looking at the configuration of the model, certain assumptions can be made to simplify it. The first would be that according to the switching pattern, without considering the cell’s capacitor being short-circuit, one cell can be ON, when capacitor is applied to the output, OFF, when the output is simply short-circuit, or in high impedance mode, when no pulses are sent to the power switches and only input voltage and the capacitor voltage determine the current. Once the current is known and whether or not it runs through the capacitor, the voltage value of each capacitor is computed as well as the output voltage of the limb. Another assumption made is that the current is the same for all cells in a limb.

As illustrated in Fig. 2, in ON and OFF mode, the current is only a function of the total circuit inductance (AC side, the DC side and the limb inductance), the cell output voltages and the source voltage. In the HighZ mode (both IGBT are OFF-mode), the output voltage of the cell is set by the voltage of its RC snubber, note that this snubber is only presented in the HighZ mode. Fig. 3 shows the eight possible modes.

In Ref. [3], a model separated on many CPU allows parallel computing that is required to achieve real-time simulation with a small time step of 20
Fig. 3 Considered behaviour of the cell.

In order to achieve a time step below one microsecond, one needs an FPGA board capable of handling a large number of I/O signals and enough computing resources to simulate each cell for all possible states. One digital-to-analog converter and two digital inputs are required per cell. It has therefore been decided to implement one MMC arm per FPGA. This way, up to 64 MMC cells could be simulated using all I/O available on the OP5142 FPGA board. The OP5142 FPGA is able to manage 64 analog output converters and 128 digital inputs, which enable the simulation of 64 cells. The number of FPGA boards required is therefore determined by the maximum number of I/O to manage and the capability of each FPGA board in terms of number of I/O channels controllable by one FPGA board.

The next challenge is to optimize the implementation of the FPGA model of each cell to make sure that all the cells could be simulated within the same FPGA chips controlling all I/Os.

One more thing to be considered is the point of connection between the different subsystems simulated on the FPGAs and on standard processors. This is even more crucial considering that both subsystems have different time step. It is common to use inductance or capacitors to separate subsystem in multi-rate real-time simulation if the variation of the inductor current and capacitor voltage is slow as compared to the time step of the simulation. But in this case the inductance has an important impact on the current computation in HighZ mode and the inductor currents and voltages have high-frequency components determined by the cell snubber. Simulation has proved that it is better to simulate this inductance on the FPGA.

This is demonstrated with a simple model, in one case the inductance is simulated with the voltage source at a time step of 20 µs and the MMC with a time step of 1 µs, Model1 in Fig. 4. Then the same model is simulated, but this time the inductance is simulated at 1 µs also, Model2 in Fig. 5.

Fig. 6-8 show the results, to understand them, one must looks at how they are simulated. For model1, the MMC cells receive the current which is determined by the output voltage of the cells, the voltage of the source and the inductance. In  this case, the values of the snubber are chosen to reduce the current close to 0, required to simulate the high impedance case when both IGBT are in OFF state. The key here is to choose a snubber value that will have a resonance frequency as high as possible to simulate actual systems but low enough to achieve numerical stability with the selected time step of 20 µs.

Of course, real snubber circuits will have rise time smaller than 20 µs, but one must accept this compromise to achieve real-time simulation required to test controllers in HIL real-time mode. Snubber circuits and fast transients across IGBT or thyristor are therefore analysed with specialized off-line simulation software such as SABER or SPICE.

In Model2, the cells receive the voltage and return the current. The current is computed based on the input voltage of the cell, voltage that would apply the
capacitor and the inductance value. In high impedance
mode, snubber time constants can then be computed at
the time step of the FPGA models, which is 20 times faster than the preceding case. This allows smaller snubber values, smaller losses and snubber values closer to the one used on real systems.

Surprisingly, one can also observe in Fig. 6-8 that both models differ by a few percentage points. This increase of accuracy for Model2 is mainly due to a more accurate simulation (solution of 1 µs instead of 20 µs) of each ON-OFF IGBT transition, which affects the charge of cell capacitors.

2.2 FPGA Modelling

When using FPGA, different approaches can be chosen because of its large versatility. This technology is well known for parallel processing enabling the simultaneous computing of many different values. The first implementation demonstrated that each cell could be simulated in less than 100 ns on the SPARTAN 3 FPGA using a 100 MHz clock. However, the number of computational resources available on the FPGA (i.e. number of adder, multipliers...) would not allow simulating up to 64 cells in one FPGA. As mentioned before, one OP5142 FPGA board can handle all the I/O required for 64 cells, but the challenge is now to simulate the 64 cells directly on the FPGA chip. Therefore, a sequential method is used that involves sharing the same FPGA resources for a group of cells. And again because of the I/O limitation, in the number available on one card, each FPGA will only compute the solution of one arm. Fig. 9 shows a block schematic of the architecture that is present on each FPGA.

In accordance with the available I/O, two limbs of 30 cells with their limbs inductance are modelled. As input, there is the AC voltage, coming from the CPU model, and the pulses sent to each cell, this signals could either be coming from an external controller or a controller also simulated on a CPU of the simulator. These gates signals are time multiplexed so the same resource is used to compute all the different capacitors voltage. Then capacitor’s voltages are demultiplexed before being sent to the CPU. The sum of the cell voltage is made and this voltage and the one coming from the source on the CPU are used to determine current in the inductance. As for output, the FPGA returns the current circulating in the limb and the capacitor voltage of each cell; these values need to be sent to the controller to allow regulation of each of them. The capacitor cells voltages are also sent on digital-to-analog converters to enable HIL simulation to use an external controller.

3. Simulation

3.1 Results

The preliminary results obtained by the simplified equivalent circuit were very good; therefore, results just as good are expected for the full model simulated with eMEGAsim [5]. The model used in this simulation is an AC/DC converter, like the one in Fig. 2 with 30 cells per limb for a total of 180 cells. No pulses are sent at the beginning, after 0.3 s pulses are generated by the MMC controller to control the power flow. 180 capacitors voltages are being monitored and individually controlled by the MMC controller to ensure that all capacitor voltages are charged to the same value. Unbalance in cell capacitor voltage will create harmonics and circulating currents. One must note here that the objective of this paper is not to demonstrate the effectiveness of a specific controller implementation but to demonstrate the accuracy of the plan simulation using the same controller.

Considering the large number of capacitor voltage monitored, the next figures only show the minimum and the maximum value of all 180 that is shown with

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Fig. 9  Block schematic of MMC model on FPGA.
the value of one of the capacitor. In Fig. 10 these capacitors voltage are shown for the model simulated at 20 µs and the one at 250 ns; both results could be superimposed. The same conclusion can be drawn from the current in Fig. 11.

The main difference is during the natural rectifying mode, when no pulses are sent. During this time, RC snubbers are used; since the value of these snubbers is determined by the time step, reducing the time step reduces the value of snubber time constant and also reduces the error introduced by snubber with large time constant. In Fig. 12, the current for the 20 µs model is much larger than the current observed with the small snubber time constant simulated at 250 ns. The arm current is about 0.02% with a simulation at 20 µs and near to zero with 250 ns. This implies that users may decide to simulate the effect of actual snubber when a simulation time step of 250 ns is used.

3.2 Total Delays for HIL Simulation and Tests

One of the critical parameters when testing actual controller and protection system performance of MMC systems is the total delay measure between IGBT firing signal transition and voltage and current outputs sent to the MMC controller. Using a time step of 20 µs, which is rather small compared to a traditional simulator achieving only 50 µs time step, will lead to a total delay of about 40 µs. A total delay of 50 to 60 µs is considered as the upper range of acceptable delay by several manufacturers. As mentioned before, this simulation with a time step of 20 µs, which yields a delay to 40 µs, is good enough to test control systems. But using FPGA based simulation with a time step of 250 ns and a

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![Fig. 10 Capacitor voltage for both models.](image1)

![Fig. 11 AC current for both models.](image2)

![Fig. 12 Current phase A for both models.](image3)
refresh of all voltage and current at each microsecond decreases the total delay to below 1 µs, which eliminates problems that could be introduced by the use of larger time step.

4. Conclusions

In this paper, results for a 250 ns time step MMC model has been presented. Such a time step is achieved using both parallel processing and time multiplexing on an FPGA.

The key advantages of FPGA-based models with very small time steps are:

1. Better accuracy for HIL simulation and tests since the resolution of firing pulse accuracy is 250 ns instead of 20 µs;
2. The total delay measured between the firing pulse transitions issued by the MMC controller and the voltage and current feedback of the simulator is reduced from 40 µs to less than 1 µs, which increases the overall accuracy considering typical MMC controller time steps of 50 µs to 100 µs;
3. Better simulation of the natural rectification mode and bloc mode (HiZ);
4. Possibility to simulate the effect of practical snubber with a time constant of 1 to 5 µs, which is impossible with a time step of 20 µs.

Furthermore, since modern simulators, such as eMEGAsim, are already equipped with FPGA boards to manage the large amount of I/O channels required by MMC, the same FPGA boards can also be used to simulate individual cells at 250 ns. Consequently, FPGA processing technology enables more accurate simulation with the same hardware otherwise needed for I/O management.

References